TSMC-02-228



October 24, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/631,842 07/31/03

Chia-Ta Hsieh

A METHOD TO FORM SELF-ALIGNED FLOATING GATE TO DIFFUSION STRUCTURES IN FLASH

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 27, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 10/27/03

U.S. Patent 6,403,494 to Chu et al., "Method of Forming a Floating Gate Self-Aligned to STI on EEPROM," discloses a method of forming a split-gate flash memory cell with the floating gate self-aligned to the shallow trench isolation (STI).

U.S. Patent 6,358,796 to Lin et al., "Method to Fabricate a Non-Smiling Effect Structure in Split-Gate Flash with Self-Aligned Isolation," teaches a method to fabricate a split-gate flash memory cell with self-aligned STI without the intrusion of a smiling gap.

U.S. Patent 6,245,685 to Sung et al., "Method for Forming a Square Oxide Structure or a Square Floating Gate Structure Without Rounding Effect," discloses a method for forming a square oxide structure or a square floating gate structure without rounding of corners.

U.S. Patent 5,688,705 to Bergemont, "Method for Reducing the Spacing Between the Horizontally Adjacent Floating Gates of a Flash EPROM Array," discloses a method for reducing the spacing between adjacent floating gates of flash memory arrays.

U.S. Patent 5,330,938 to Camerlenghi, "Method of Making Non-Volatile Split Gate EPROM Memory Cell and Self-Aligned Field Insulation," discloses a method of making a non-volatile split-gate EEPROM cell with self aligned field insulation.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

# INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)



| Docket Number (Optional) | Application Number |
|---|---|
| TSMC-02-228 | 10/631,842 |
| Applicant: Chia-Ta Hsieh | |
| Filing Date: 07/31/03 | Group Art Unit: |

## U. S. PATENT DOCUMENTS

| Examiner Initial | Document Number | Date | Name | Class | Subclass | Filing Date if Appropriate |
|---|---|---|---|---|---|---|
| | 6,403,449 | 6/11/02 | Chu et al. | 438 | 719 | 8/14/00 |
| | 6,358,796 | 3/19/02 | Lin et al. | 438 | 257 | 4/15/99 |
| | 6,245,685 | 6/12/01 | Sung et al. | 438 | 719 | 9/1/99 |
| | 5,688,705 | 11/18/97 | Bergemont | 437 | 43 | 8/21/96 |
| | 5,330,938 | 7/19/94 | Camerlenghi | 437 | 57 | 6/18/93 |
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## FOREIGN PATENT DOCUMENTS

| | Document Number | Date | Country | Class | Subclass | Translation YES | Translation NO |
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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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| EXAMINER | DATE CONSIDERED |
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.